



Atty. Docket No. 8041-1011

PATENTS

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Koji FURUSAWA

Confirmation No. 3216

Serial No. 09/939,761

GROUP 2815

Filed August 28, 2001

Examiner Edgardo Ortiz

SEMICONDUCTOR DEVICE

RESPONSE

Commissioner for Patents

Washington, D.C. 20231

Sir:

This responds to the Official Action of October 30, 2002. Claims 7-21 are present in the application.

Claims 7, 8, 12, 14, 15 and 17 are rejected as unpatentable over TAKIAR et al. 5,502,289 in view of SHINOHARA 5,238,878. This rejection is respectfully traversed.

Claim 7 of the present application recites a wiring layer between first and second semiconductor chips, the wiring layer including a polyimide tape having a copper foil layer therein, wherein the second semiconductor chip is mounted on the wiring layer by an adhesive material and the wiring layer is provided on the first semiconductor chip without using an adhesive material.

By way of example, Figures 3 and 4 of the present application show a wiring layer between first and second semiconductor chips 2, 3. As disclosed on page 7, lines 16-19 of the present application, in the embodiment shown in Figure 3, the